Course syllabus

IC-projekt 1
IC-project 1

ETIN35, 7,5 credits, A (Second Cycle)

Valid for: 2023/24
Faculty: Faculty of Engineering, LTH
Decided by: PLED E
Date of Decision: 2023-04-11

General Information

Compulsory for: MSOC1
Elective for: D4, E4-is
Language of instruction: The course will be given in English

Aim

The aim is to provide knowledge about practical design of integrated circuits, with an emphasis on system-on-chip. The circuits can be either analog, digital, computer oriented, or mixed mode, and the design work can be performed on either transistor or block level.

Learning outcomes

Knowledge and understanding
For a passing grade the student must

- have knowledge about modern CAD-tools for integrated circuit design
- understand the design process from specification to finished circuit
- have knowledge about the limitations of the technology chosen

Competences and skills
For a passing grade the student must

- be able to design an integrated circuit using CAD tools according to a given specification
- be able to make a time plan according to a given time frame
- be able to present his/her results in oral as well as written form

Judgement and approach
For a passing grade the student must

- feel familiar in a modern design environment for integrated circuits
- be able to read and understand a specification and to handle the design process all the way to a finished integrated circuit

Contents

The design of integrated circuit is a rapidly growing field which has a large need of well educated engineers. The course is performed as a project work, where the students in small groups apply their knowledge from earlier courses to design an integrated circuit (IC=Integrated Circuit), also known as a chip. This is done using modern CAD tools. Several projects can be performed so that they can be connected together creating a larger system.

The course provides the students a unique opportunity to design a complete chip, where a number of selected designs can be submitted to fabrication at the end of the project work. The manufacturing of the selected designs takes about 3 months, after which they are verified in the course IC-project continuation and verification.

The ambition is that the main part of the project should have a broad content with parts that are analog, mixed mode, and digital parts. Such a project can have different groups designing the different parts.

The digital part also contains a number of mandatory parts to make the students acquainted with the CAD-tools needed to perform the project.

Examination details

Grading scale: TH - (U,3,4,5) - (Fail, Three, Four, Five)
Assessment: The grade is based on the quality of the project work as well as the report and oral presentation of the work. The work is performed in groups and an assessment is made of the efforts of the group as well as the individual participants. If the work is not finished within the given regular time frame, a higher grade than 3 can not be given. The students who perform a digital project must first pass a number of hand-in exercises and have them approved before the project part of the course starts. There will be an extra opportunity to pass the hand-in assignments the first Monday in VT2.

The examiner, in consultation with Disability Support Services, may deviate from the regular form of examination in order to provide a permanently disabled student with a form of examination equivalent to that of a student without a disability.

Parts
Code: 0118. **Name:** Project.
Credits: 6. **Grading scale:** TH. **Assessment:** presentations **Contents:** Approved project
Code: 0218. **Name:** Assignment.
Credits: 0. **Grading scale:** UG. **Contents:** RTL coding and ASIC flow
Code: 0318. **Name:** Report.
Credits: 1,5. **Grading scale:** UG. **Assessment:** Approved report **Contents:** project results

Admission

Admission requirements:

- ETIN25 Analog IC Design (analogue) or EITN20 Digital IC Design and EITF35 Introduction to Structured VLSI Design (digital) or EITF20 Computer Architecture and EITF35 Introduction to Structured VLSI Design (computer)

The number of participants is limited to: No
The course overlaps following course/s: ETIN01, ETI210

Reading list

- Course material will be available on the homepage of the course.

Contact and other information

Course coordinator: Baktash Behmanesh (analog), baktash.bemanesh@eit.lth.se
Course coordinator: Liang Liu, liang.liu@eit.lth.se
Course homepage: http://www.eit.lth.se/course/etin35