Course syllabus

Digitala strukturer på kisel Introduction to Structured VLSI Design

EITF35, 7,5 credits, G2 (First Cycle)

Valid for: 2023/24
Faculty: Faculty of Engineering, LTH
Decided by: PLED E
Date of Decision: 2023-04-11

General Information

Main field: Electronic Design.
Compulsory for: MSOC1
Elective for: D4-is, D4-hs, E4-is
Language of instruction: The course will be given in English

Aim

- General introduction to large-scale digital integarted circutis design with emphasis on FPGA implementation
- Efficient design-flow using modern CAD tools
- Design methodology for synchronous logic
- Modeling with synthesizable VHDL
- Rapid prototyping using FPGA

Learning outcomes

Knowledge and understanding
For a passing grade the student must

- Know how to perform synchronous design
- Be well-versed in conventional VHDL modeling
- Have tasted from the test, diagnose

Competences and skills
For a passing grade the student must

- Be skilled in logic synthesis & physical mapping using state-of-the-art design tools

Judgement and approach
For a passing grade the student must

- have a first “idea to product” experience

Contents

The course consists of the following four main parts: 1) Design flow based on modern design tools, 2) Use of VHDL as design language and input for logic synthesis, 3) Design of synchronous systems by developing clock cycle true models, 4) Use of field programmable gate arrays (FPGA) for rapid prototyping.
The course contains lectures and poejects (including preparations). The projects are design oriented and based on the use of tools for simulation, synthesis, and optimisation with FPGA as the target technology.

Examination details

Grading scale: TH - (U,3,4,5) - (Fail, Three, Four, Five)
Assessment: Oral examination of 3-5 projects. Grade depends on the number of projects that have been completed by the course deadline. A re-exam will consist of an extra project in addition to the regular projects and at least 2 weeks will be given to complete this. A re-exam will always be offered after the Christmas break.

The examiner, in consultation with Disability Support Services, may deviate from the regular form of examination in order to provide a permanently disabled student with a form of examination equivalent to that of a student without a disability.

Admission

Assumed prior knowledge: EITF65 Design of Digital Circuits OR EITA35 Electronics OR EITF90 Electromagnetics and Electronics
The number of participants is limited to: No
The course overlaps following course/s: EIT120

Reading list

- Chu: Rtl Hardware Design Using Vhdl. John Wiley And Sons Ltd, 2006, ISBN: 9780471720928.

Contact and other information

Course coordinator: Liang Liu, liang.liu@eit.lth.se
Course homepage: http://www.eit.lth.se/course/eitf35