LUNDS UNIVERSITET
Lunds Tekniska Högskola

Course syllabus

Digitala system
Digital Systems

EITA15, 15 credits, G1 (First Cycle)

Valid for: 2023/24
Faculty: Faculty of Engineering, LTH
Decided by: PLED C/D
Date of Decision: 2023-04-18

General Information

Compulsory for: IDA1, IEA1
Language of instruction: The course will be given in Swedish

Aim

The aim of the course is to give the engineer fundamental knowledge in digital technique and in computer technique. The purpose is also to give practical skills in structured methods of solving problems, of construction and of seeking failure in equipments.

Learning outcomes

Knowledge and understanding
For a passing grade the student must

- be able to explain Boolean algebra and binary arithmetic
- be able to describe the function of combinational networks and of sequential networks
- be able to describe the principles of how a computer works at register level
- be able to apply systematic methods of analysis and synthesis of combinational and sequential networks.

Competences and skills
For a passing grade the student must

- be able, by programming (in the language of VHDL and C), to design a digital system consisting of programmable chips or of embedded systems
- be able in writing, to document a construction made in VHDL or in C
- have the fundamental knowledge to in the future, as an working engineer, incorporate and learn new low level programming languages.

Contents

- Logical algebra. Boolean algebra. Modulo-2 algebra
- Binary arithmetic. Number systems. Binary codes. 2-complement and 10-complement
- Combinational networks. Simplification and application of Boolean functions in a gate network. Karnaugh maps. Standard gate networks for the application of Boolean functions
- Fundamental sequential networks. Counters, registers and shift registers
- Sequential networks. The concept of state. Sequential network models, e.g. Mealy and Moore. Synchronized and non-synchronized sequential networks. Latches and Flip-flops
- Hardware descriptive language VHDL. Introductory concepts in VHDL. Description of a small combinational network in VHDL
- Semiconductor memory. Memory models. Classification of semiconductor memories. Read-only memories. Address decoding. Read/write memories, RWM, static and dynamic memories
- Digital/analoge – analoge/digital converter
- The computer model: the computer's parts and functions. The CPU at the register level
- Assembly programming
- Program development in C: editing, compilation, linking. Testing with the aid of a high level debugger.
- The project involves carrying out a minor construction independently, reporting verbally and documenting the result in a written report.

Laboratory exercise will provide in-depth training in the subject and highlight the following:

The connection to those elements dealt with in digital systems.

- Gates in MOS technology
- Hazard and critical race
- Programmable logical circuits. Classification of integrated circuits
- Description of sequential and combinational networks in VHDL. Structural description at block level
- Application of combinational and sequential networks in programmable logical circuits
- Program development in C: problem structuring. Program components. Programming technology for embedded systems.
- Parallel ports. Serial ports. A/D conversion. D/A conversion
- Interrupt systems: periodical interrupts. Priority during interrupts. Drive routines
- The computer as a system component: Interface technology. Single board computers. Microcontrollers
- The development of computer technology: History. Developmental trends.

Examination details

Grading scale: TH - (U,3,4,5) - (Fail, Three, Four, Five)
Assessment: Written exam, approved laboratory work in computer engineering and digital engineering, approved assignments/dugga and approved projects containing design and written report.

The examiner, in consultation with Disability Support Services, may deviate from the regular form of examination in order to provide a permanently disabled student with a form of examination equivalent to that of a student without a disability.

Parts

Code: 0119. **Name:** Written Exam.
Credits: 4,5. **Grading scale:** TH. **Assessment:** Passed written exam. **Contents:** Written Exam

Code: 0219. **Name:** Laboratory Work, Digital Systems.
Credits: 3. **Grading scale:** UG. **Assessment:** Passed laboratory experiments. **Contents:** Laboratory experiments in Digital Systems.

Code: 0319. **Name:** Laboratory Computer Systems.
Credits: 2. **Grading scale:** UG. **Assessment:** Passed laboratory experiments. **Contents:** Laboratory experiments in Computer Systems. **Further information:** For participation in the laboratory of computer engineering, it is necessary to complete the laboratory of digital engineering.

Code: 0419. **Name:** Home Assignments.
Credits: 2,5. **Grading scale:** UG. **Assessment:** Passed Home Assignments. **Contents:** Home Assignments.

Code: 0519. **Name:** Project.
Credits: 3. **Grading scale:** UG. **Assessment:** Passed Project with Construction and written Report. **Contents:** Project

Admission

The number of participants is limited to: No
The course overlaps following course/s: EDI601, EDT603, EDI610

Reading list

- Föreläsningsanteckningar. Will be available at course web page.
- Technical manuals.
- Laboratory material will be handed out as the course progresses.

Contact and other information

Course coordinator: Erik Larsson, erik.larsson@eit.lth.se
Course homepage: http://www.eit.lth.se/course/eita15